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13. ABSTRACT *(Maximum 200 words)*

We realized that achieving 10 ns resolution would still require significant time interleaving and would be based on the rather complicated ECL semiconductor technology, which introduces additional risk. We decided instead to make more time-resolution advances in several smaller steps, so that the robustness, functionality, and flexibility could be enhanced in systems we could easily test. The 4.5 GHz transient digitizer already contains mature high-speed electronics and only requires a trigger signal with small jitter, which can readily be achieved with conventional CMOS technology. Time resolutions below 1 ns seem therefore possible.

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Final Report
AFOSR Grant #F49620-96-1-0322
Event-locked Time-resolved Fourier Spectroscopy for ns dynamic processes

Robert E. Peale

University of Central Florida
10 September 1997

Work under this grant on Event-locked Fourier Spectroscopy (ELFS) resulted in the following publications, patent, and presentations. Copies are included with this report.

Papers

1. "Event-locked Time-Resolved Fourier Spectroscopy", H. Weidner and R. E. Peale, Applied Spectroscopy 51 (1997), to appear.

2. "Transient event-locked Fourier spectrosocpy,", H. Weidner and R. E. Peale, J. Luminescence **72-74**, 1020 (1997).

3. "Spectroscopy of Er^{3+} in K_2YF_5," R. E. Peale, H. Weidner, F. G. Anderson, and N. M. Khaidukov, OSA TOPS Vol. 10 Advanced Solid State Lasers, 1997 Clifford R. Pollock and Walter R. Bosenberg (ed.), (Optical Society of America, Washington D.C.), pp 462-466.

4. "Quality analysis for least-squares transformation of unevenly spaced interferograms," H. Weidner and R. E. Peale, submitted Applied Spectrosc. 1997.

Presentations

1. International Conference on Luminescence, Prague, August 1996.
2. OSA annual meeting, Rochester, October 1996.
3. Advanced Solid State Lasers, Orlando, January 1997.
4. *Fourier Transform Spectroscopy, Santa Fe, February 1997.*
5. Invited Seminar, Environmental Molecular Sciences Lab, Pacific Northwest National Lab
6. Fourier Transform Spectroscopy, Athens, Georgia, August 1997.
7. Invited Talk, OSA Annual Meeting, Long Beach, October 1997
8. Invited Colloquium, Department of Chemistry , Texas A&M, October 1997

United States Patent Application

"Event Locked Continuous-Scan Fourier Spectroscopy,", Inventors: Robert E. Peale and Henry Weidner, for the University of Central Florida, mailed 1/17/97.

Next is presented a description of each milestone in the development of Event-locked Fourier spectroscopy (ELFS). Details on the technique and representative results are found in the enclosed publications. At the end is a description of future plans, for which there is currently no funding.

ELFS10

This precurser to Event-locked Fourier spectroscopy was developed to avoid gross errors caused by mirror speed spikes. It was essentially an improved version of the classic interleaved method and hence is not really ELFS at all. It caught desynchronizations in which different numbers of samples per reference fringe occur, and it repeated those mirror scans. Interferograms were transformed by usual FFT.

Fig. 1 presents photographs of the electronics, including a digital board and analog board housed in a rack mounted cabinet external to the spectrometer and computer. Commercial counter/digital-I/O and 98 kHz 16 bit ADC boards were housed in a PC.

ELFS20

Event-locked data acquisition and speed recording is introduced here for the first time. The same 16 bit 98 kHz ADC is used giving a time resolution of 1 μs with factor 11 time-interleaving. An arbitrary channel gain queue was implemented to allow use of a reference detector. The ELFS transform method was implemented for the first time.

The digital board was redesigned to allow speed recording and ELFS acquistion. This board was thenceforth designated the "Process Synchronizer." Through-hole printed circuit boards were designed and manufactured inhouse using discrete logic chips. Photographs of the boards used are presented in Fig. 2.

ELFS20 demonstrated the feasibility of ELFS. Weaknesses were revealed and studied and ideas for enhancing functionality, flexibility, and robustness were generated. This system formed the basis for our patent application.

ELFS3x

AFOSR support under grant #F49620-96-1-0322 began here. ELFS3x was developed as two subversions, which differed in time resolution. ELFS31 used the old 16 bit 98 kHz ADC giving 1 μs resolution by interleaving 11 time delays. ELFS32 used a Computer Boards 12 bit 1 MHz ADC to obtain 200 ns resolution with a time-interleaving factor of 5. ELFS32 was the first commercially successful version of Event-Locked Fourier Spectroscopy. A copy of our prototype was sold to NRC Canada for semiconductor research at a price of $10000 by the start-up Zaubertek, Inc. Zaubertek has licensed the technology from the University of Central Florida, who will hold the patent. Bomem, Inc. has published an application note on ELFS32 and plans to sell versions manufactured by Zaubertek to its DA3/8 users for $15000. The cost increase will cover installation, support, and license fee.

Besides increasing the time resolution, ELFS3x introduced a number of important improvements. The Process Synchronizer was redesigned to be more robust, to use surface mount electronics, to reside internal to the PC, and to have more built-in flexibility. It introduced filtered inputs to protect againts noise, reduced cabling, and removed the need for a rack-mounted container.

In ELFS3x, the analog board was still external to the PC and spectrometer, but in a small box. The software still ran under DOS. Even though the Process Synchronizer was internal to the PC, it did not use the PC bus. Photographs of the electronics for ELFS31 and ELFS32 are presented in Figs. 3 and 4, respectively.

ELFS40

This project was begun in May 97 and completed in August 1997. The Process Synchronizer is now a true plug-in card using the PC bus signals. A programmable logic device (PLD) replaces the discrete logic chips for extra speed and flexibility. The counter card has been eliminated because its function is assumed by the Process Synchronizer. The extra speed makes

100 ns resolution possible using a time-interleaving factor of 10.

Extra features are introduced to facilitate experiments. A built-in spectrum analyzer is included to help track down electrical noise sources. A built-in oscilloscope is included so that pulse forms can be viewed directly at the computer. The program now runs as a Windows95 application.

FFT analysis is included in addition to the patented ELFS procedure, because it is faster and was found numerically to be adequate for interogram point unevenness less than 20% (see preprint). Exact analysis of the ELFS formulas is included, although it is very slow, for situations where the highest quality is required.

An external analog box is still used to power the detectors and provide gain. Fig. 5 presents photographs of the system.

ELFS50

ELFS50 is a fully designed future version and is presented in Fig. 6. Implementation depends on funding. A 14 bit, ≥2.5 MHz, ADC chip will be added to the Process Synchronizer to eliminate the separate ADC board. Former functions of the ADC board will be assumed by a larger PLD, including the channel gain queue and sample buffers. A time resolution of 50 ns will be possible with a time interleaving factor of 8. The external analog box will be eliminated by including its function on the single printed circuit board to facilitate high speed data paths. Inputs on the board will have a zero shift to better use the dynamic range of the ADC, which will eliminate the present requirement for special detector preamps. Ribbon cables will eliminated in favor of double-shielded coax with SMA connectors for high speed and noise suppression.

Other Future Plans

If funding is available, we plan to implement the ELFS technique on an industry grade Bomem MB FTIR borrowed from Kennedy Space Center. This will allow the technique to be used by a much wider group of scientists, engineers, and perhaps even in industrial process control. The MB allows access to both transmitted and reflected beams of the Michelson interferometer. The phase relation of these two signals allows the uninteresting DC component to be subtracted while adding the modulated components. Then the gain can be increased to make best use of the ADC. Optimal use of the ADC will reduce the necessary bits to 8 while maintaining a dynamic range better than 11 bits with increased speed but little increase in cost. The great range in possible gain allowed by DC subtraction will allow filling of the 8 bit ADC at all path length differences.

Funding was received recently from DURIP/BMDO/AFOSR for mode-locked THz laser research, and a 4.5 GHz digitizer has been acquired. Using it instead of the ADC will permit a time resolution of 100 ps.

Another plan is to enhance the use of ELFS for measuring time-dependent transmittance, where relative changes are small.

Where activities differed from the proposal

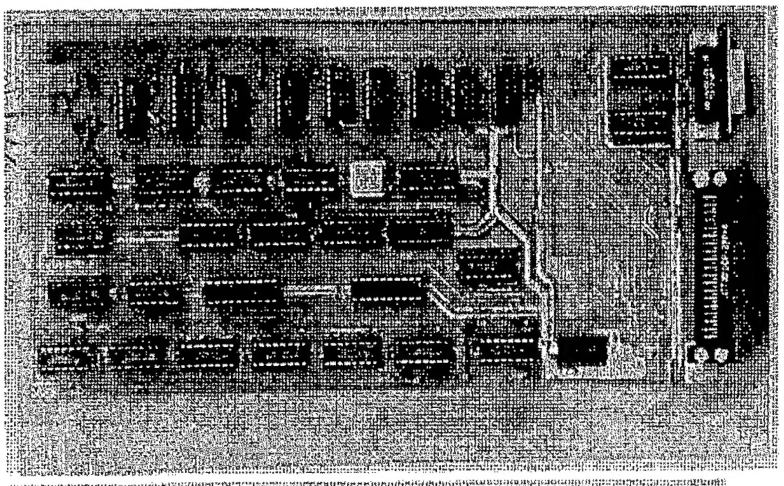
We originally planned to jump from 200 ns to 10 ns resolution by using dual 30 MHz ADCs with interleaved channels for $8000. We realized that achieveing 10 ns resolution would still require significant time interleaving and would be based on the rather complicated ECL semiconductor technology, which introduces additional risk. We decided instead to make more time-resolution advances in several smaller steps, so that the robustness, functionality, and flexibility could be enhanced in systems we could easily test. The 4.5 GHz transient digitizer already contains mature high-speed electronics and only requires a trigger signal with small jitter, which can readily be achieved with conventional CMOS technology. Time resolutions below 1 ns seem therefore possible.

Educational activities

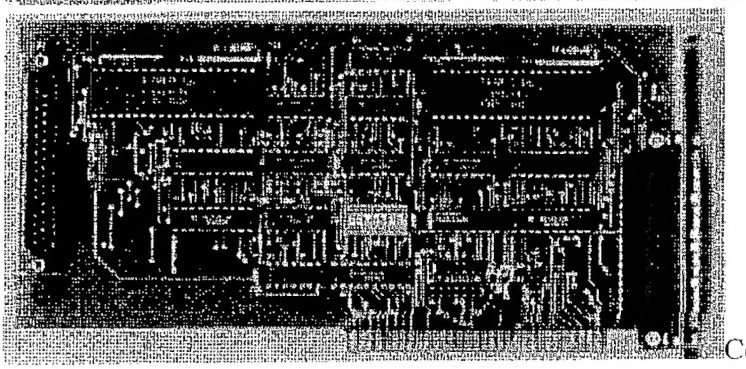
Henry Weidner will defend his PhD thesis this semester.

ELFS10:

FIG. 1

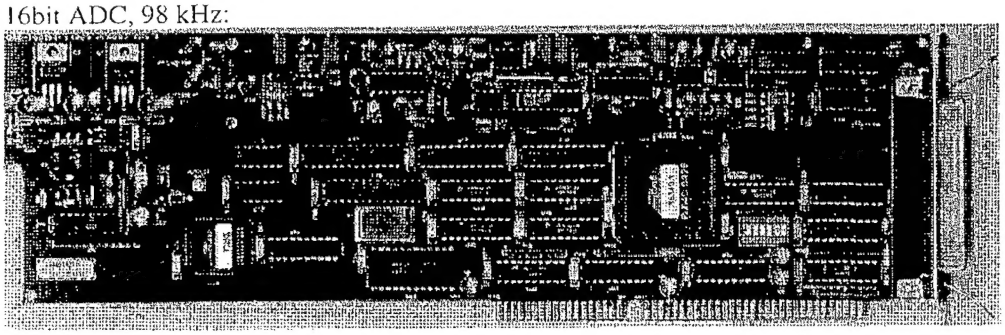


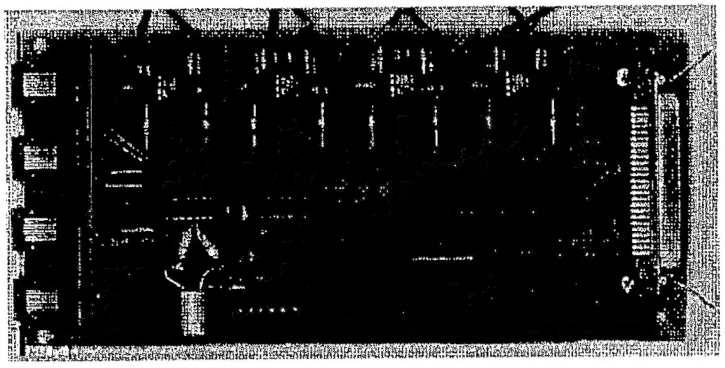
Digital board



Counters and digital in/output

16bit ADC, 98 kHz:

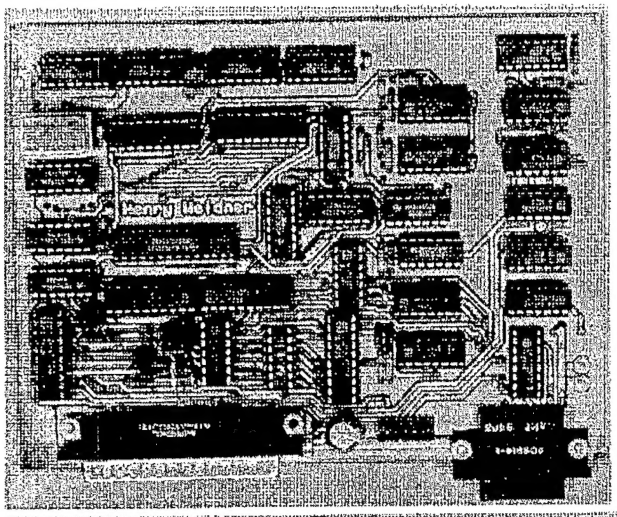




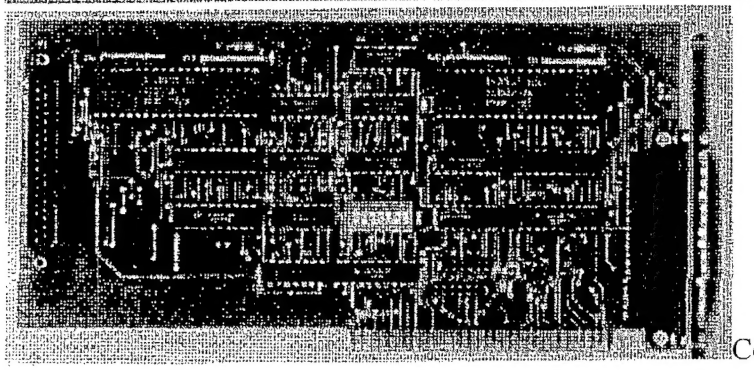
Analog board

FIG. 2

ELFS20:

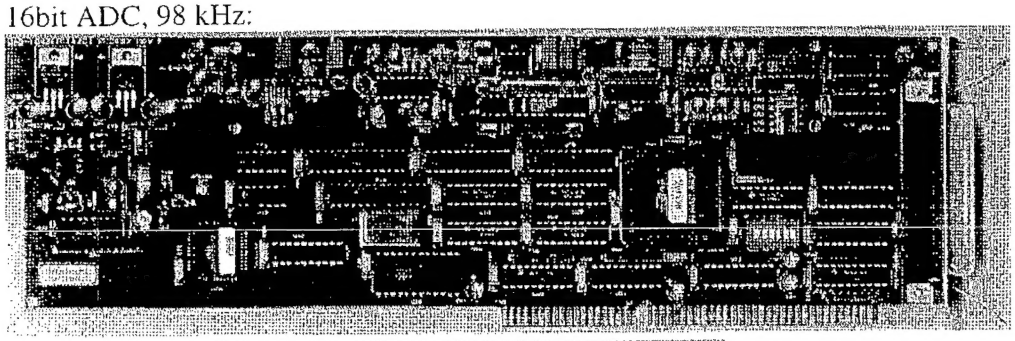


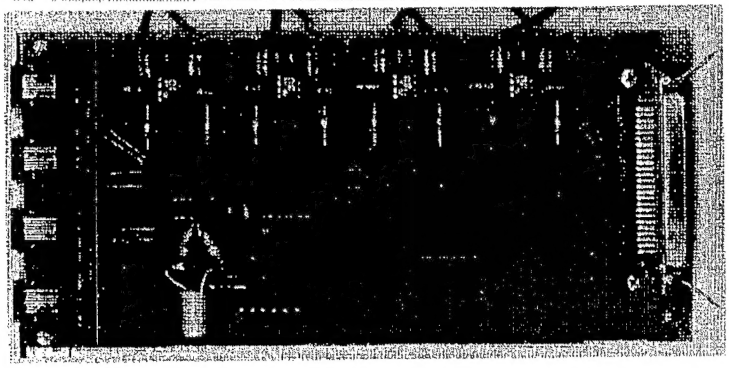
Process synchronizer



Counters and digital in/output

16bit ADC, 98 kHz:



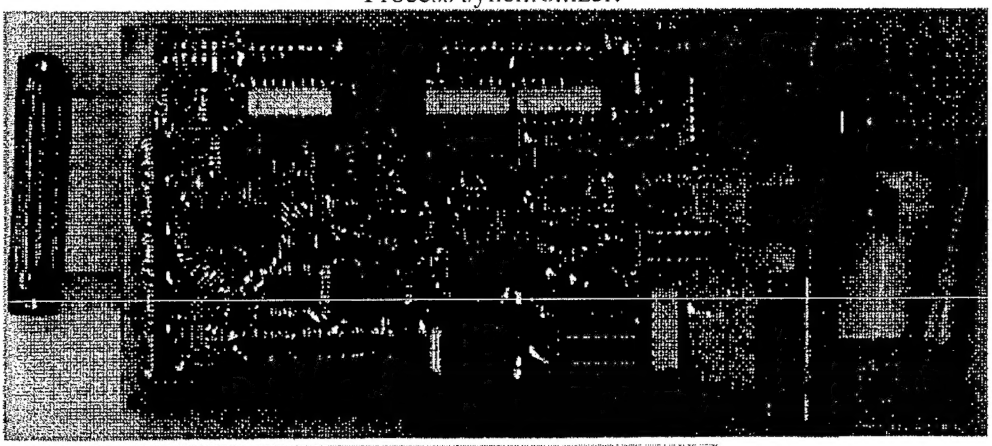


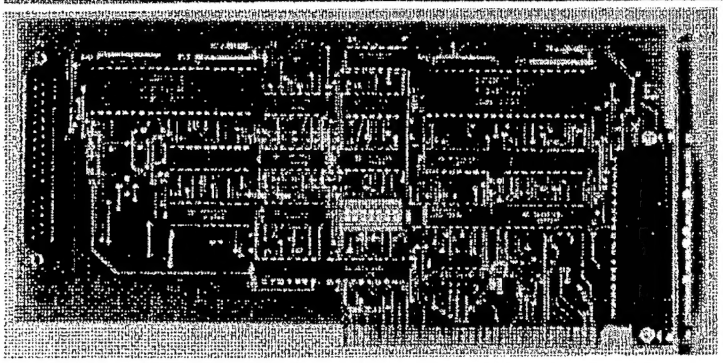
Analog board

ELFS31:

FIG. 3

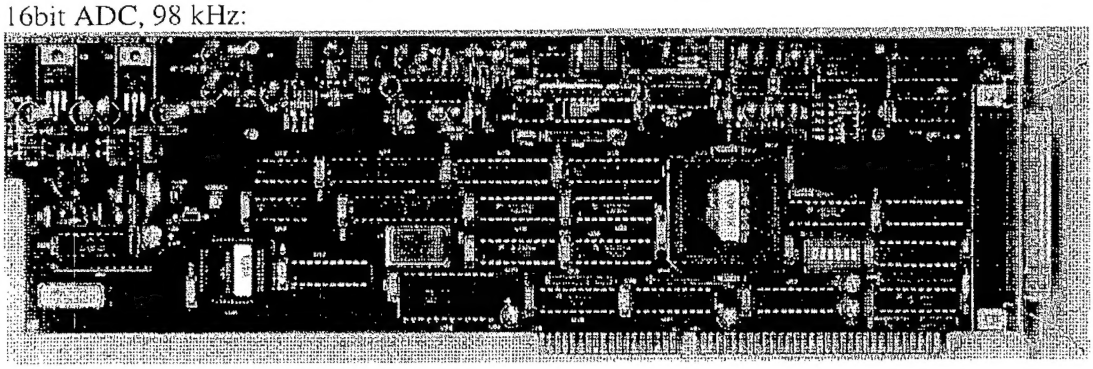
Process synchronizer:

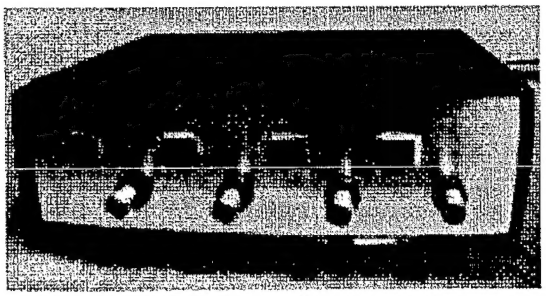




Counters and digital in/output

16bit ADC, 98 kHz:



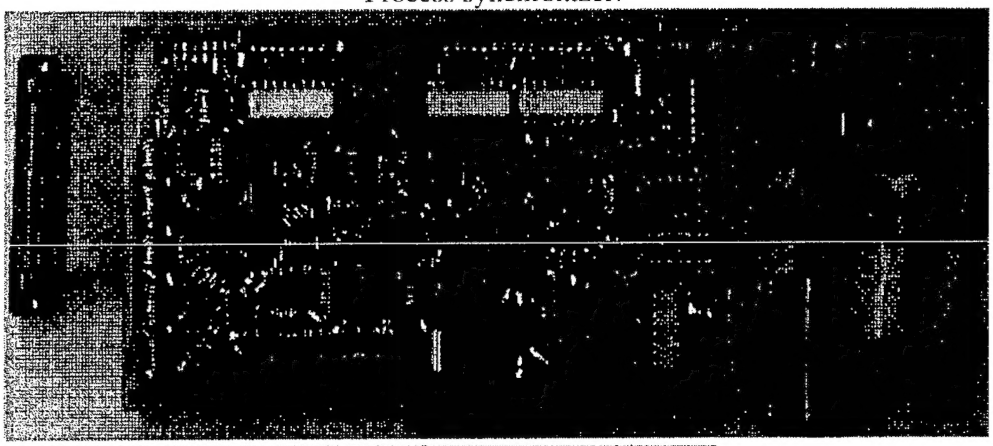


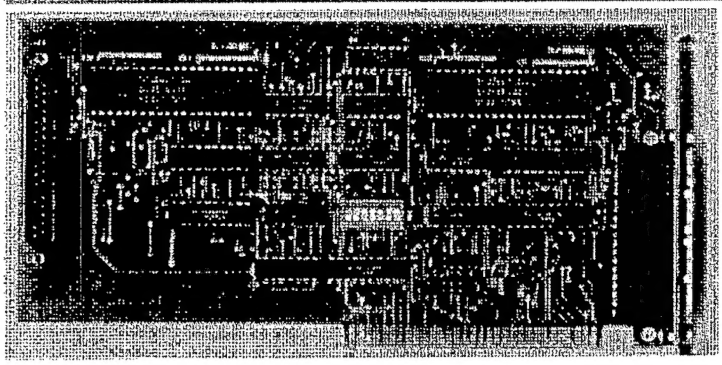
Analog box

FIG. 4

ELFS32:

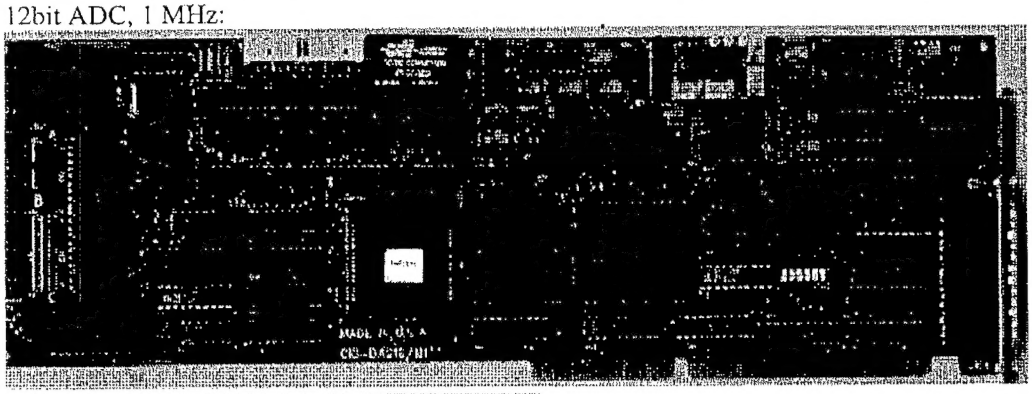
Process synchronizer:

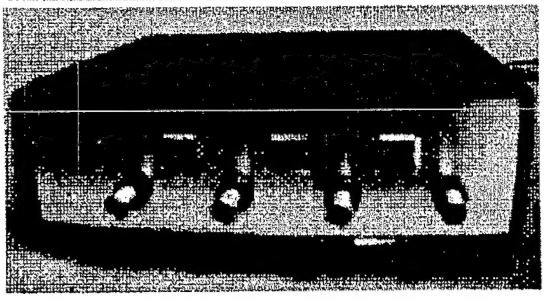




Counters and digital in/output

12bit ADC, 1 MHz:



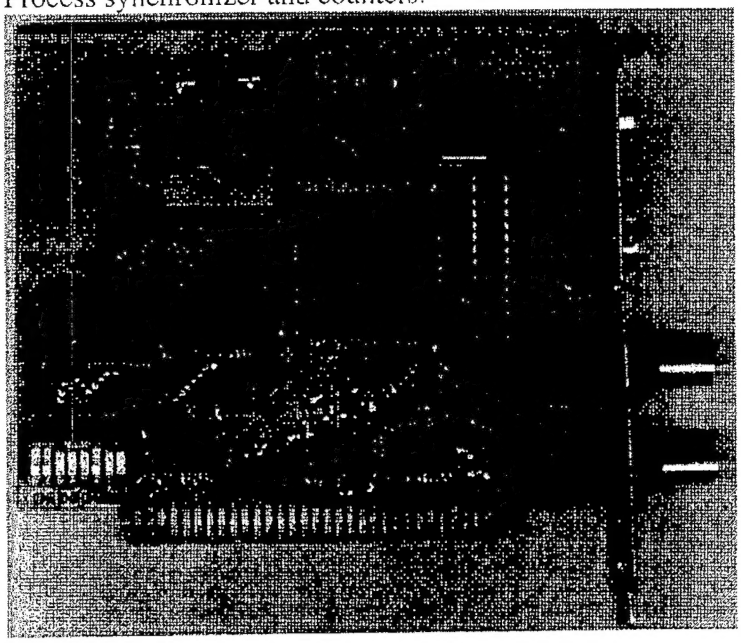


Analog box

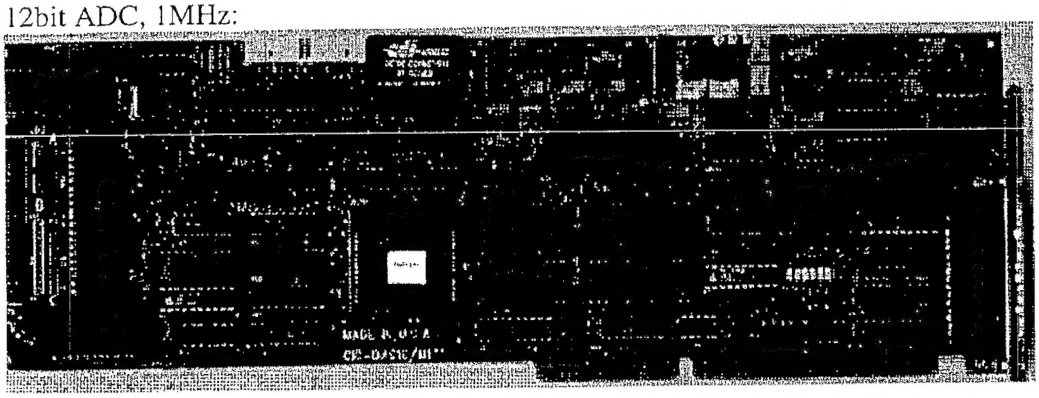
ELFS40:

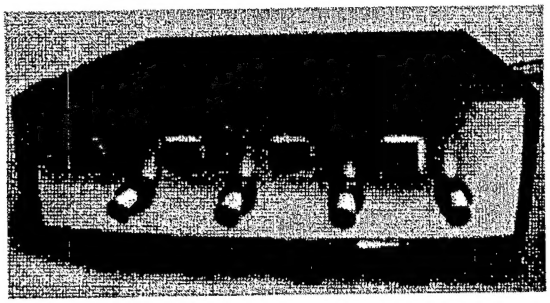
FIG. 5

Process synchronizer and counters:



12bit ADC, 1MHz:





Analog box

ELFS50:

FIG. 6

only one board: